

**Department of Electrical and Electronic Engineering**

**EE4011 – RF IC Design**

**Preliminary Report**

**Summary of Research Paper on an RFIC Topic:**

**A Dual Front-End for the New GPS/GALILEO Generation in a 0.35 μm SiGe Process**

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# 1. Operation of the GPS/Galileo System

The Global Positioning System (GPS) is a Global Navigation Satellite System (GNSS) which transmits radio waves signals that can be picked up by GPS receivers on earth to determine location and synchronised time. It is being maintained by the United States government. The current GPS system is based on 24 satellites located in six orbital planes at a height of 20,200 km circling the earth every 12 h. Each satellite has two ranging codes, the Coarse/Acquisition (C/A) code freely available to the public and a restricted Precision (P) code used by the military.

The C/A code is a pseudorandom noise (PRN) code which is transmitted at 1.023 Mbit/s and repeats itself every millisecond. The satellites all have unique PRN codes which are highly orthogonal with each other. This is a form of code division multiple access (CDMA) which allows all the satellites to transmit at the same frequency and the receiver can differentiate individual satellite codes. The P code is also a PRN code except that it is transmitted at 10.23 Mbit/s and repeats itself once a week. This extreme length increases its correlation gain and eliminates range uncertainty.

For ranging codes to be transmitted from the satellite to the receiver they must be modulated onto a carrier frequency. The original GPS system has two carrier frequencies, L1 (1575.42 MHz) and L2 (1227.6 MHz). The C/A code is transmitted on the L1 frequency while the P code can be transmitted on both the L1 and L2 frequencies. Both codes are transmitted using a bi-phase shift keying (BPSK) modulation technique.

Along with the ranging codes the GPS satellites also send a navigation code which contains information about each satellite’s position and the network. The navigation message is made up of three parts. The first part contains the GPS date, time and the satellite’s status and an indication of its health. The second part, called the ephemeris data, contains the orbital information used to calculate the position of the satellite. The third part, called the almanac data, contains the coarse location and PRN numbers of all the satellites. The almanac data assists the receiver in deciding which satellites to look for. When a satellite is then found the receiver downloads the ephemeris data directly from that satellite.

The US Department of Defense (DoD) is currently renewing the GPS satellite system and 29 new satellites are being launched between 2003 and 2012. These new satellites aim to improve accuracy and availability for all users. There are several new signals foreseen for GPS, L2C, L1C and L5. The L2C is transmitted on the L2 frequency and will be used to transmit the C/A signal for civilian use. The effect of having two civilian frequencies will allow civilian receivers to measure the ionospheric delay error and cancel its effect. The ionospheric error is due to the delay that the navigation signals suffer when they travel through the ionosphere. This delay, if not corrected, can lead to large positioning errors. The L1C is transmitted on the L1 frequency using a Binary Offset Carrier (BOC) (1,1) modulation technique. The L1C signal allows greater civil interoperability with Galileo L1. The L5 signal is a civilian safety of life signal with a frequency of 1176.45 MHz.

The Galileo system will consist of 30 satellites positioned in three circular Medium Earth Orbit planes at 23,616 km altitude above the Earth. The frequencies used by the satellites are in the 1.1 – 1.6 GHz band. Each Galileo satellite will broadcast 10 different navigation signals allowing four services to be offered by Galileo: Open Service (OS), Safety-Of-Life (SOL), Commercial (CS) and Public Regulated services (PRS). Figure 1 shows the frequency spectrum of the Galileo system. Due to the large number of signals that the Galileo system has, there are several combinations for ionospheric cancellation. Single frequency services (L1, E5a, E5b or E5a and E5b together) with the error being removed using a model, dual frequency services (L1 and E5a can be used for the best ionospheric error cancellation as cancellation is more effective for larger separation between the two frequencies) and triple frequency services using all the signal together (L1, E5a and E5b) which can be used for very precise centimetric applications.

From Figure 1 it can be seen that there are two coincident frequency bands where both systems send navigation messages available for civil users: the GPS L1 with the Galileo E1-L1-E2 and the GPS L5 with the Galileo E5a. The distinctive modulation shape of the Galileo signals has been chosen to avoid interference with other satellite navigation systems such as the GPS L1 signal in this case. The modulation used is BOC (1,1) which allows the GPS and Galileo signals to occupy the same frequency while avoiding mutual interference. This makes building receivers that can use both GPS and Galileo possible where they will be able to deliver the position of one or both systems at the same time.

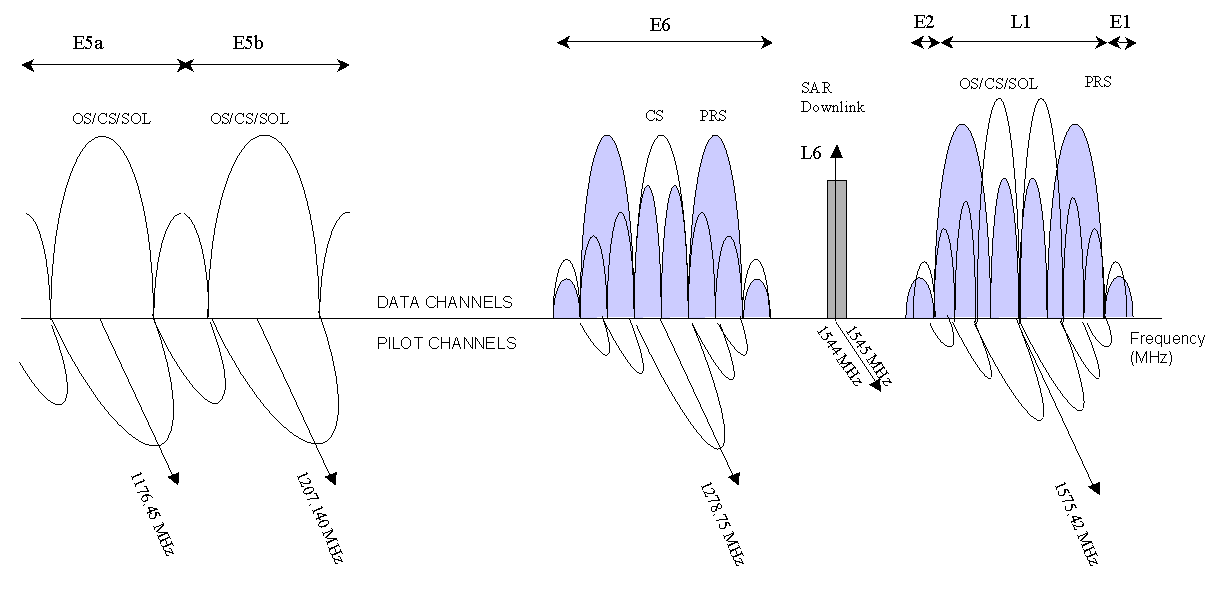


Figure : Galileo Frequency Spectrum

# 2. IC Receiver Specifications

The RF IC receiver aims to design an RF front-end that receives the GPS L1 and Galileo E1-L1-E2 signal frequencies so the receiver can deliver the position of one or both systems at the same time. The following are the specifications of the GPS/Galileo receiver.

## 2.1 Gain

The system requires a high gain due to weak incoming signals received from the satellites. The minimum gain spec is 93 dB for an estimated ADC offset lower than 25 mV and input impedance higher than 4 kΩ.

## 2.2 Noise Figure and Sensitivity

The GPS has a C/No ratio of 46 dB/Hz at the input of the antenna. The minimum C/No to the input of the demodulator is 27 dB/Hz. Therefore the maximum Noise Figure (NF) of the RF front end is 17 dB. The Galileo has a C/No ratio of 46 dB/Hz at the input of the antenna and therefore has a maximum NF of 16 dB. However the lower the NF of the receiver the better sensitivity, accuracy and acquisition time it has because the detection probability increases and the signal integration time decreases. A maximum NF of 3.5 – 4 dB has therefore been specified for the RF front-end.

## 2.3 Linearity

Due to the low variance of power received by the antenna, linearity specifications are not critical. However linearity becomes a key parameter when considering the performance of the receiver against an external jammer. Figure 2 shows the maximum allowable interference power at different frequencies around the L1 frequency that will allow a correct demodulation of the signal. It can be seen that the minimum maximum power allowed occurs at the L1 frequency of 1575.42 MHz.

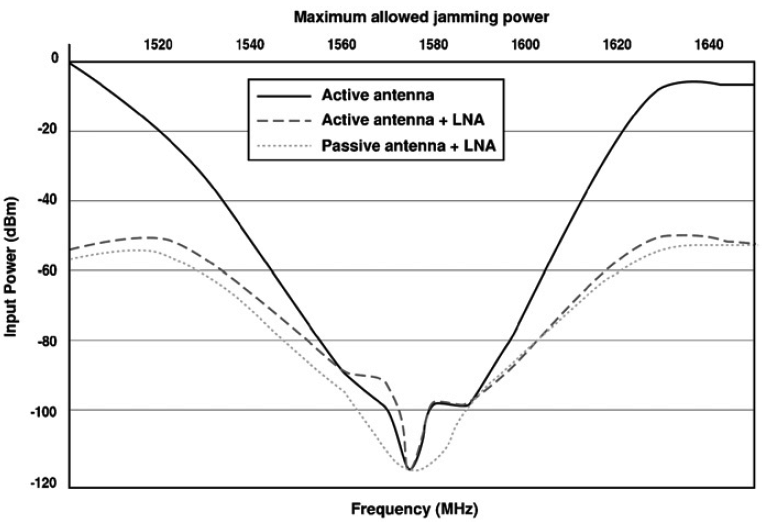


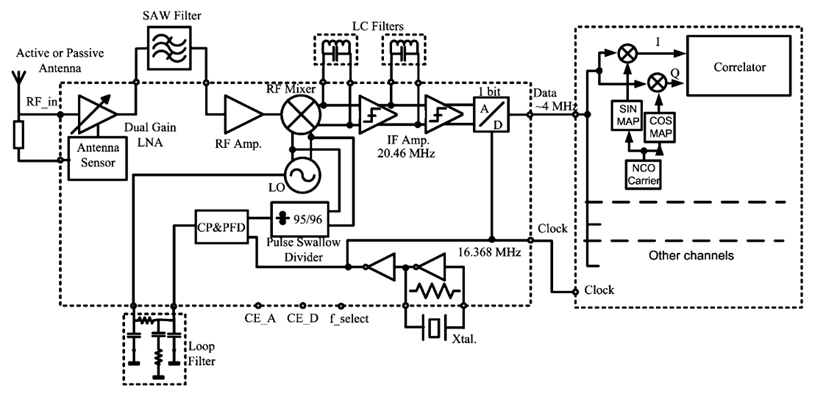
Figure : Maximum allowable interference power at different frequencies that will allow a correct demodulation of the signal

## 2.4 Bandwidth:

The bandwidth of the Galileo E1-L1-E2 signal is 24 MHz compared to the 2.046 MHz bandwidth of the GPS. It is possible to have the bandwidth of the receiver narrower than Galileo without high degradation of the C/No. It was found that the degradation due to pre-correlation filtering of the Galileo BOC (1,1) signal for a 6 MHz bandwidth filter is only 0.5 dB. Therefore the bandwidth spec has been set to 6 MHz.

# 3. IC Block Diagram and Description

Figure 3 shows the block diagram of the receiver. It consists of a 1. dual-gain LNA (Low Noise Amplifier) with an integrated antenna sensor, a Surface Acoustic Wave (SAW) filter for removing the image signal, a (2) RF amplifier and mixer which have been joined in one to optimise gain and power consumption, (3) a highly integrated Phase-Locked Loop (PLL) with an external loop filter and quartz crystal, (4) an IF amplifier with external LC filters and 5. a 1-bit analogue to digital (A/D) convertor. The four critical elements of the receiver are the dual-gain LNA, RF mixer, PLL and the 1-bit ADC.



**1**

**2**

**3**

**4**

**5**

Figure : Block Diagram of the Receiver

## 3.1 Dual-Gain LNA

The dual gain LNA has been designed with an integrated antenna sensor to sense the presence of a passive or active antenna. This will help avoid the risk of early receiver loading due to unwanted interference. Figure 4 shows a schematic of the inductively generated LNA. In the inductively generated LNA schematic, transistors Q1 and Q2 and degeneration inductors form the input stage. In high gain mode transistors M1 and M2 are selected and Rload = R1||(R1+R3) while M3 and M4 are turned off. In low gain mode transistors M3 and M4 are selected and Rload = R2||(R1+R3). The output of the LNA consists of a common collector stage which performs the on-chip output impedance matching.

In the antenna sensor and gain selection circuit as shown in Figure 5, the antenna sensor stage detects whether the antenna is passive or active by sensing the voltage drop Rant due to the power consumption of the antenna. This creates a voltage Vcont which sets the control voltage for the gain selection stage. If the voltage drop across Rant is large, Vcont will be large thus turning on transistor M2, turning off Q4 and causing V\_LO to go to low. Similarly V\_HI will be high thus turning on M1 and M2 in the LNA circuit and turning off M3 and M4.

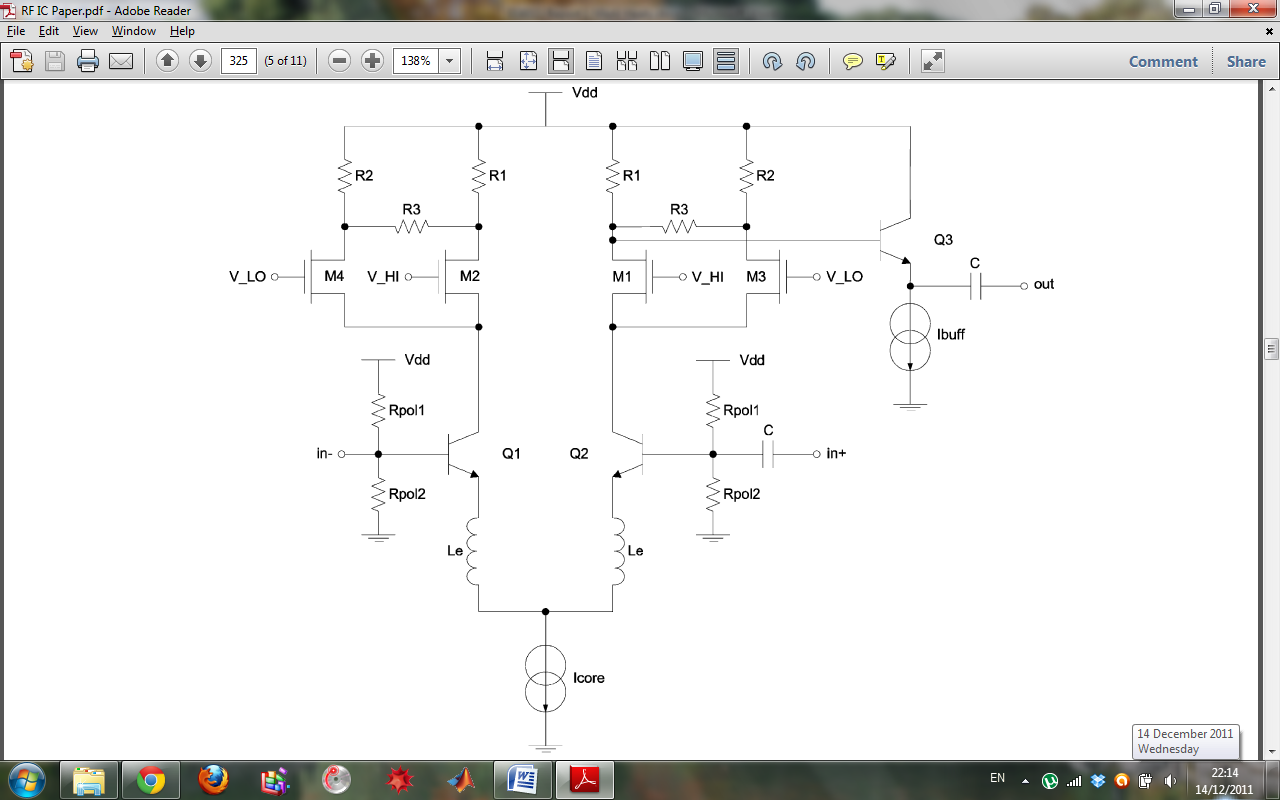


Figure : Schematic of inductively degenerated LNA

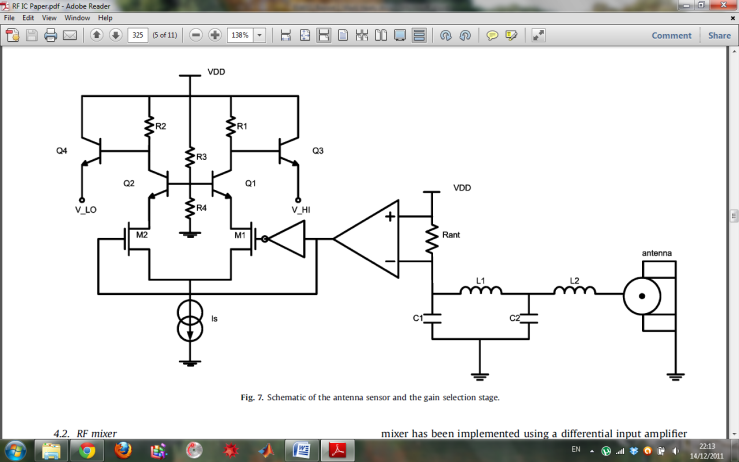


Figure : Schematic of antenna sensor with gain selection stage

The general circuit design was understandable but some of the finer details such as the effect of the degeneration inductors were not known. LNA design using Smith charts has been discussed in class.

## 3.2 RF Mixer

Figure 6 shows the schematic for the RF mixer. It consists of a differential input amplifier for a relatively high gain receiver configuration and a Gilbert cell which is used an analogue multiplier and frequency mixer to produce the IF frequency. The RF output from M1 and M2 of the differential amplifier connected to the gate of Q3 and Q4 of the Gilbert cell, the Local Oscillator (LO) output is connected to the gate of Q5, Q6, Q7, Q8 and the IF output is being taken from the collector of Q6 and Q7. The input impedance of the Gilbert cell has been fixed in order to optimise power consumption, gain, NF and linearity of the entire RF mixer.

The load of the preceding amplifier will be higher due to higher input impedance of the Gilbert cell and therefore no extra power is need to increase the gain of the RF amplifier keeping power consumption low. To suppress the LO signal at the IF output, a differential Gilbert cell and external filtering are used.

The area where I felt least prepared is how the circuit is optimised for power consumption, gain etc. by having fixed impedances and relatively high impedances for different parts of the circuit. We have not covered Gilbert cells in EE4011 to date.

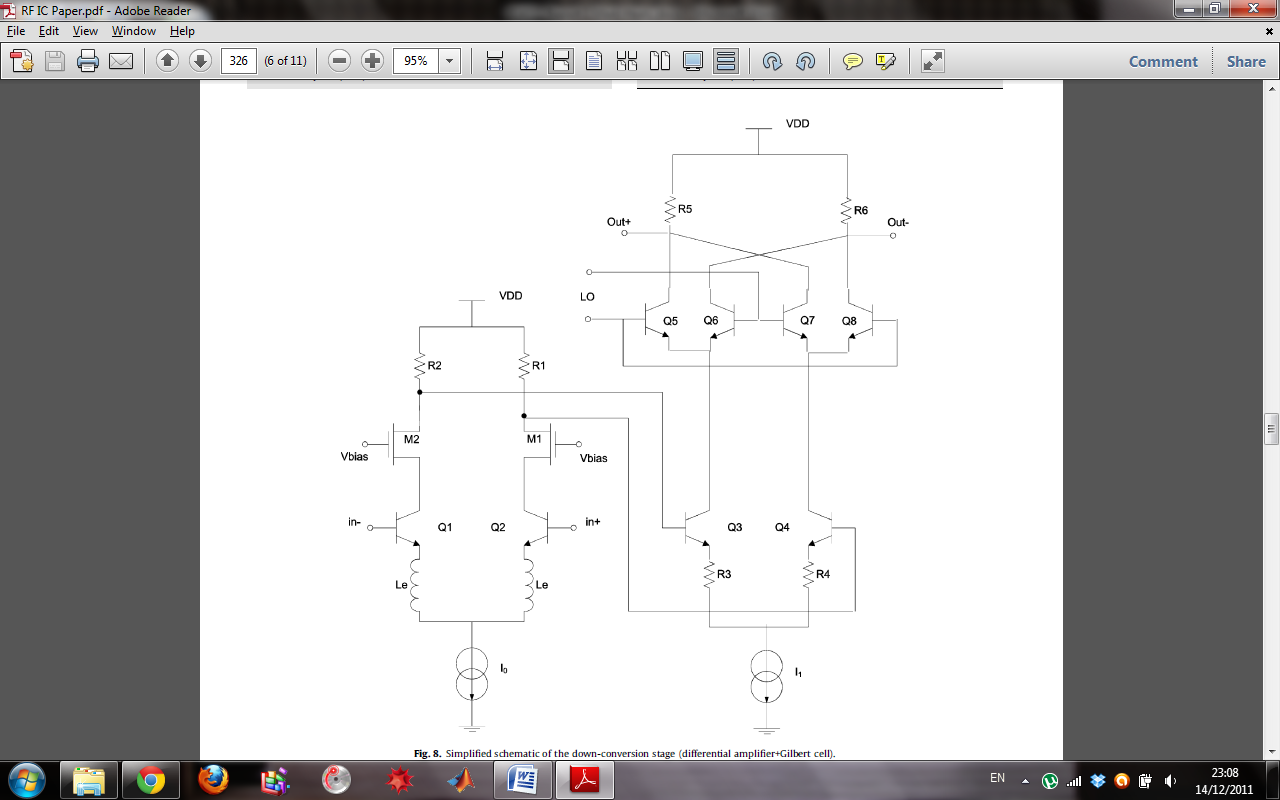


Figure : Simplified schematic of the down conversion stage (differential amplifier+Gilbert cell)

## 3.3 Phase Locked Loop (PLL)

Figure 7 shows the block diagram of the PLL. The PLL must provide frequencies the two 1554.69 and 1571.328 MHz which are created using the pulse swallow divider which can divide the oscillator frequency by 95 and 96. The pierce oscillator creates a reference frequency which is compared to the output of the phase swallow divider in the phase frequency detector (PFD) circuit. The PFD circuit detects the difference in the two frequencies and creates an error signal used to correct the frequency of the VCO. The output of the PFD controls the charge pump which sets the tuning voltage of the Voltage-Controlled Oscillator (VCO) through the loop filter. The output of the VCO is AC coupled into the RF mixer and also back into the pulse swallow divider to create a feedback loop for closed loop control of the VCO.

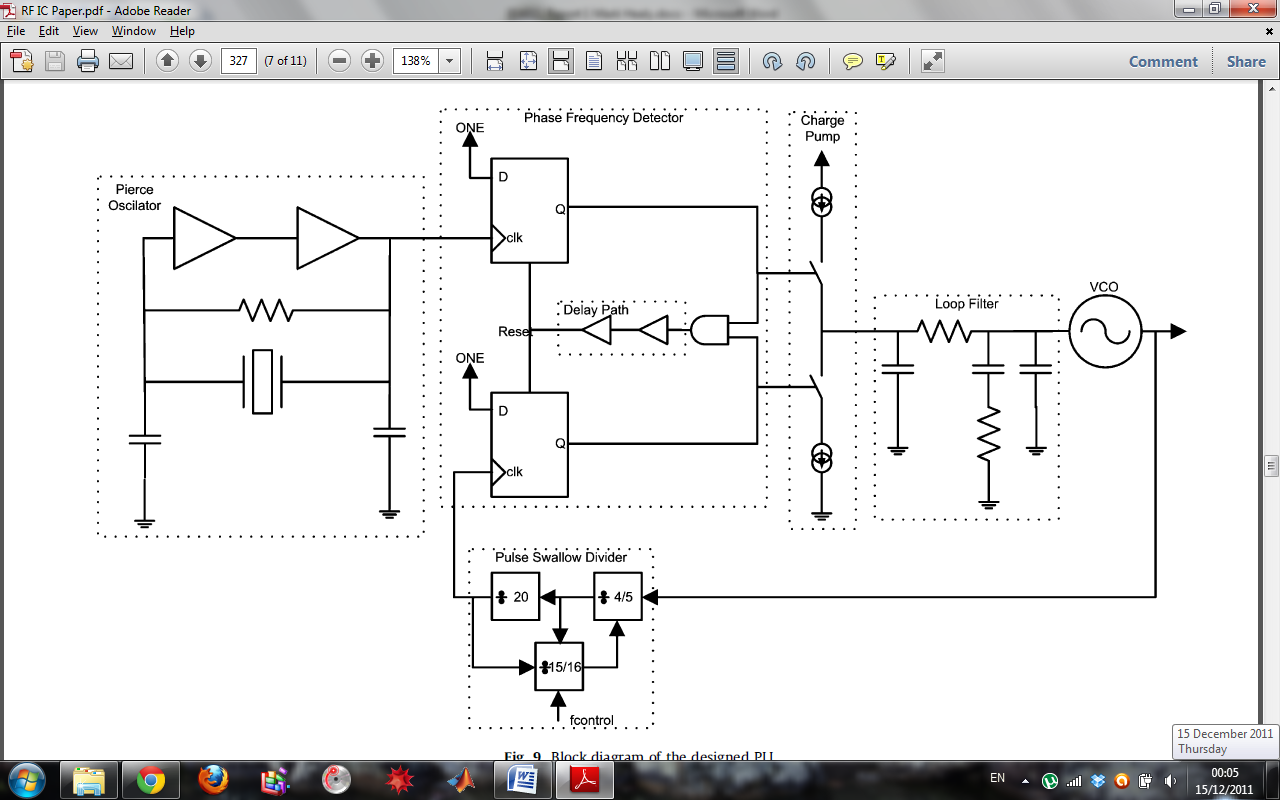


Figure : Block Diagram of the PLL design

shows a simplified schematic of the VCO. The LC VCO is implemented using a cross-coupled configuration with a high Q fully integrated LC tank. This way power consumption of the oscillator can be minimised while keeping phase noise performance.

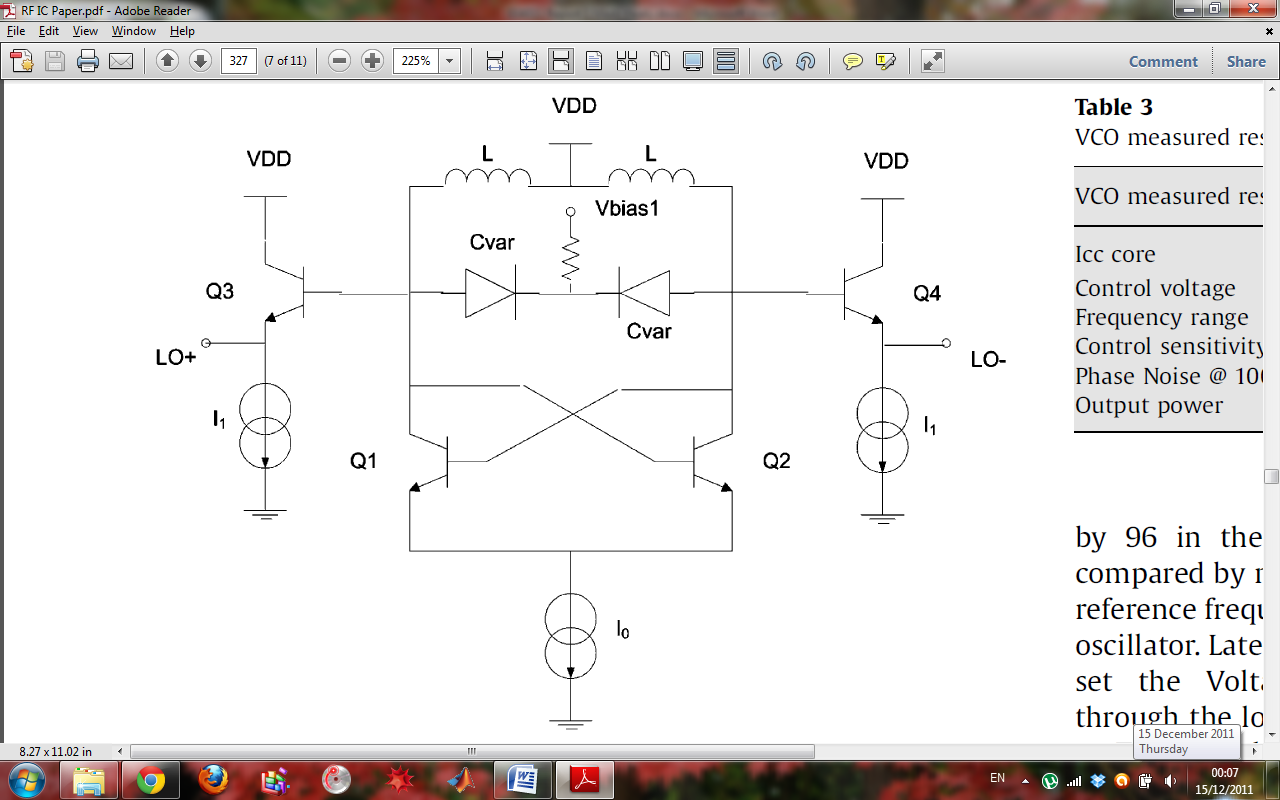


Figure : Simplified schematic of the Voltage Controlled Oscillator (VCO)

While a general understanding of the PLL and the interaction of its inner blocks is known, the inner workings of the individual block such as the Pierce oscillator, PFD, loop filter, VCO and pulse swallow divider are not known. The Pierce oscillator, PFD, VCO and pulse swallow divider circuits have not been covered in the EE4011 class to date.

## 3.4 1-bit A/D convertor

A 1-bit A/D convertor was implemented using a latch as shown in Figure 9. The A/D convertor is used to convert the IF signal into a digital signal where it is then sent to a second chip where signal detection is performed using signal processing. The A/D convertor is sampled using the Pierce oscillator frequency of 16.638 MHz. This down converts the incoming IF signal to a frequency of 4.092 MHz. Using a 1-bit A/D convertor slightly degrades the performance compared to a multi-bit convertor but results in a simpler, lower power receiver without automatic gain control.

The operation of a Analogue to Digital Convertor (ADC) is known but the exact working of the latch circuit is not. Latch circuits have not yet been covered in EE4011.

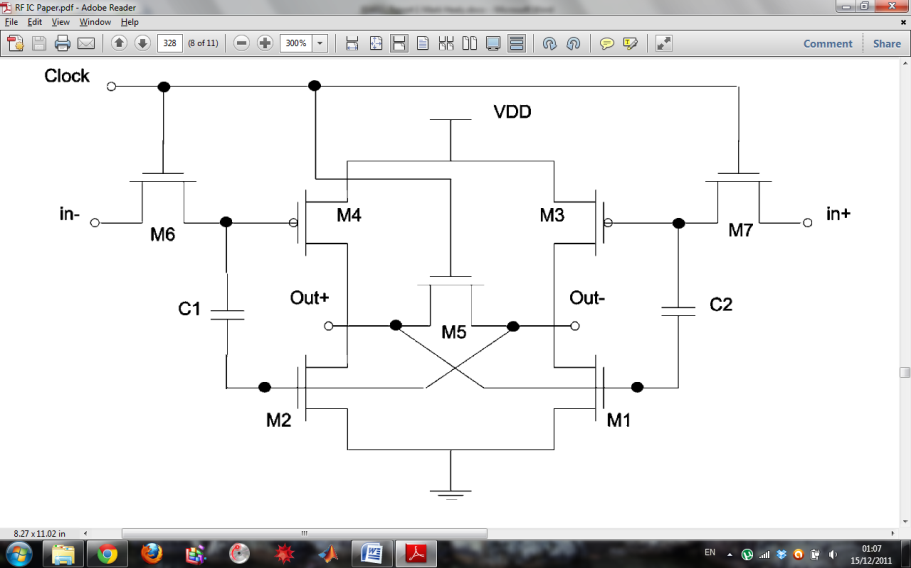


Figure : Latch Schematic

# 4. Further Study of Specific Block

The main block of the RF IC receiver that I would like to investigate further is the phase locked loop (PLL) block. I would like to investigate the PLL as a whole or possibly one of its sub blocks such as the Pierce oscillator circuit, phase frequency detector circuit or the Variable-Controlled Oscillator (VCO) circuit.

The reason I would like investigate the PLL or one of its sub-blocks is because I find it the most interesting part of the RF IC. It is the block that I know the least and it has not been covered in our previous three years at college. It is the largest of the block in the IC and has the most complicated circuit design due to its vast size. I think I will gain the most by investigating the PLL block as it is the block that I have the least knowledge of, and to me, appears to be the most complex. I am interested to learn how the PFD detects and corrects the frequency difference, how the VCO can change its output frequency using a control voltage and how the Pierce oscillator uses a crystal to create a consistent and accurate frequency signal. Also this block has an element of control in it which is another area of engineering that I am very interested in.

# Bibliography

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